January 6, 2006

METROPOLITAN STATE COLLEGE *of* DENVER
Office of Academic Affairs

REGULAR COURSE SYLLABUS

School of: Letters, Arts, and Sciences

Department: Mathematical and Computer Sciences

CIP Code: 11.0701

Prefix & Course Number: CS 3400 **Crosslisted With*:** _____

Course Title: Computer Architecture

Check All That Apply: Required for Major: _____ Required for Minor: _____ Specified Elective: _____
Required for Concentration: X Elective: X Service Course: X

Credit Hours: 4 (4 + 0)

Total Contact Hours per semester (assuming 15-16 week semester):

Lecture 60 Lab 0 Internship 0 Practicum 0 Other (please specify type and hours): 0

Schedule Type(s): Lecture **Grading Mode(s):** Letter

Variable Topics Courses (list restrictions, including the maximum number of hours that can be earned**):

_____

** **NOTE: This information must be included in the course description.**

Restrictions (Variable Topics Course): _____

Prerequisite(s): CS 2050 and CS 2400 with grades of "C" or better, or permission of instructor

Corequisite(s): None

Prerequisite(s) or Corequisite(s): _____

Banner Enforced:

Prerequisite(s): _____
Corequisite(s): _____
Prerequisite(s) or Corequisite(s): _____

Catalog Course Description:

Computer architecture concepts are extended to include advanced architectural concepts based on the quantitative analysis and evaluation of modern computing systems. These include advanced instruction set architecture designs, multilevel and set associative caches, advanced pipelining, out-of-order processors including superscalar and VLIW techniques, microprogramming concepts, multiprocessing architectures, advanced memory organizations, input/output, and network-oriented interconnections.

APPROVED:

Ruth G. Yarar — 1-17-06
Department Curriculum Committee — Date

Steve Beaty — 1/19/06
Department Chair ~~OR Program Director~~ — Date

Dal Lansky — 1/31/06
Dean **OR** Associate Dean — Date

Associate VP, Academic Affairs — Date

*If crosslisted, attach completed Course Crosslisting Agreement Form

Prefix and Course Number: CS 3400 January 6, 2006

Required Reading and Other Materials will be equivalent to:

Computer Architecture: a Quantitative Approach, 2nd edition, Hennessey and Patterson, Morgan Kaufman, 1996

Specific, *Measurable* Student Behavioral Learning Objectives:
Upon completion of this course the student should be able to:

1. Discuss and compare the performance of alternative design choices in system design.
2. Qualitatively describe the reasons for performance differences in the levels of an advanced memory hierarchy.
3. Use quantitative analysis and evaluation of modern computing systems.
4. Perform performance computations.
5. Describe the principal instruction pipelining concepts.
6. Analyze the dependencies in a program and explain how dynamic or static rescheduling can reduce the pipelining stalls.
7. Describe the memory hierarchy.
8. Describe the principal protection models.
9. Describe the differences among direct, set associative and fully associative cache organizations and address mapping.
10. Using locality of reference principles, qualitatively describe performance issues associated with virtual memory organization.
11. Explain cache block and virtual memory page replacement approaches.
12. Describe context switching.
13. Explain interconnection networks and clusters and perform queuing theory calculations.
14. Explain network topology, internetworking principles, and clustering of PCs.
15. Describe the three major methods of I/O data transfer.
16. Describe asymmetric multiprocessing hardware and symmetric shared-memory multiprocessors.
17. Describe the issues of synchronization.
18. Explain memory consistency models.
19. Describe super computer parallel processing concepts.

Detailed Outline of Course Content (Major Topics and Subtopics):

I. Fundamentals of Computer Architecture
   A. Components of computer architecture: instruction set architecture, computer organization, IC technology.
   B. Performance measuring
   C. Classifying instruction set architecture, memory addressing
   D. RISC and CISC approaches

II. Advanced Pipelining
   A. Instruction level parallelism
   B. Data hazards
   C. Control hazards
   D. Structural hazards
   E. Exploiting instruction-level parallelism with software and hardware approaches
   F. Multiple instruction issue in superscalar and VLIW architectures

III. Memory Hierarchy Design
   A. Physical memory: SRAM, DRAM, ROM, EPROM;
      1. Memory organization;
      2. Memory addressing;
      3. Direct memory access.

B. Cache memory:
   1. Multilevel caches;
   2. Set associative cache vs. direct mapped cache;
   3. Write thru vs. write back cache
   4. Coherency.

C. Virtual memory
   1. Physical to virtual address conversion;
   2. Memory management;
   3. Protection of virtual memory.

D. Secondary and tertiary storage systems
   1. RAID;
   2. CS storage;
   3. Network attached storage;
   4. Storage area network
   5. File system performance.

IV. Advanced Input/Output Organization
   A. I/O data transfer methods
   B. Polled, Interrupt driven, Block transfer
   C. I/O channels and DMA

V. Multiprocessing and Multicomputers
   A. Shared memory architectures
   B. Models of memory consistency
   C. Massive parallel systems
   D. Clusters of workstations

Evaluation of Student Performance:

1. Homework and Programming assignments
2. Quizzes and Examinations
3. Final Examination
4. Research Papers and/or Book Reports
5. Oral Presentations

As determined by the instructor. Written communication skills will be applied in this course.