METROPOLITAN STATE COLLEGE *of* DENVER
Office of Academic Affairs

REGULAR COURSE SYLLABUS

School of: Professional Studies

Department: Engineering Technology

CIP Code: 15.0303

Prefix & Course Number: EET 4020 **Crosslisted With*:** _____

Course Title: Digital Circuits III - Hardware Description Language

Check All That Apply: Required for Major: _____ Required for Minor: _____ Specified Elective: X

Required for Concentration: _____ Elective: X Service Course: _____

Credit Hours: 3 (2+2)

Total Contact Hours per semester (assuming 15-16 week semester):

Lecture 30 Lab 30 Internship _____ Practicum _____ Other (please specify type and hours):_____

Schedule Type(s): B **Grading Mode(s)**: L

Variable Topics Courses (list restrictions, including the maximum number of hours that can be earned**):

____

** **NOTE: This information must be included in the course description.**

Restrictions (Variable Topics Course): _____

Prerequisite(s): (EET 2350 or CSS 2227 or permission of instructor) and EET 3330 with grades of "C" or better

Corequisite(s): _____

Prerequisite(s) or Corequisite(s): _____

Banner Enforced:

Prerequisite(s): (EET 2350 or CSS 2227) and EET 3330 with grades of "C" or better
Corequisite(s): _____
Prerequisite(s) or Corequisite(s): _____

Catalog Course Description:
This course covers a Hardware Description Language (HDL) which is used to design and simulate very large scale digital integrated circuits.

APPROVED:

Department Chair **OR** Program Director	1 May 08 Date
Dean **OR** Associate Dean Kathy Utley	5/5/08 Date
Associate VP, Academic Affairs Richard Wagner	12/17/08 Date

*If crosslisted, attach completed Course Crosslisting Agreement Form

Prefix and Course Number: EET 4020

Required Reading and Other Materials will be equivalent to:

Palnitkar, Samir (2003). *Verilog HDL 2nd edition* or current edition. Upper Saddle Hill, NJ: Prentice Hall

Specific, *Measurable* Student Behavioral Learning Objectives:
Upon completion of this course the student should be able to:

1. Use a Hardware Description Language (HDL) to emulate hardware logic gate operation, establish data flows, and model desired logic behavior.
2. Simulate hardware designs using HDL and verify the results.
3. Synthesize and test designs on Programmable Logic Device (PLD) hardware.

Detailed Outline of Course Content (Major Topics and Subtopics) **or Outline of Field Experience/Internship (experience, responsibilities and supervision):**

I. Gate, Dataflow and Behavioral Level Modeling and Simulation
   - A. Combinatorial Circuits
   - B. Registered Logic Such as Registers and Counters
   - C. Finite State Machines

II. Simulation and Testing Designs
   - A. Waveform simulation
   - B. Writing Test Benches with HDL
     1. HDL Programming Structures for Simulation
     2. Topics in Verification and Simulation

III. PLD Synthesis of HDL designs
   - A. Synthesis Tools and Writing Efficient Logic for the PLD
   - B. Timing Closure
   - C. Constraints Management

IV. Course Projects
   - A. Implement a Logic Design Project
   - B. Verify Operation with Simulation
   - C. Demonstrate Operation to the Class

Evaluation of Student Performance:

1. Lab Reports
2. Written Exams
3. Assignments
4. Presentations