METROPOLITAN STATE COLLEGE *of* DENVER
Office of Academic Affairs

REGULAR COURSE SYLLABUS

School of: Professional Studies

Department: Engineering Technology

CIP Code: 15.0303

Prefix & Course Number: EET 3330 **Crosslisted With*:** _____

Course Title: Digital Circuits II

Check All That Apply: Required for Major: X Required for Minor: X Specified Elective: _____

Required for Concentration: _____ Elective: _____ Service Course: _____

Required for Certificate: X

Credit Hours: 3 (2+2)

Total Contact Hours per semester (assuming 15-16 week semester):

Lecture 30 Lab 30 Internship _____ Practicum _____ Other (please specify type and hours):_____

Schedule Type(s): B **Grading Mode(s)**: L

Variable Topics Courses (list restrictions, including the maximum number of hours that can be earned**):

_____

**** NOTE: This information must be included in the course description.**

Restrictions (Variable Topics Course): _____

Prerequisite(s): EET 2310 with a grade of "C" or better

Corequisite(s): _____

Prerequisite(s) or Corequisite(s): _____

Banner Enforced:

Prerequisite(s): EET 2310 with a grade of "C" or better
Corequisite(s): _____
Prerequisite(s) or Corequisite(s): _____

Catalog Course Description:
This course is a continuation of EET 2310. It covers the analysis and design of sequential (counters and shift registers) logic circuits. Programmable Logic Devices (PLD) and associated Computer Aided Design (CAD) software are used to implement digital circuits using the schematic design entry method.

APPROVED:

Department Chair **OR** Program Director	1 May 08 Date
Dean **OR** Associate Dean	5/5/08 Date
Associate VP, Academic Affairs	12/17/08 Date

*If crosslisted, attach completed Course Crosslisting Agreement Form

Prefix and Course Number: EET 3330

Required Reading and Other Materials will be equivalent to:

1. Hamblen, James O., Hall, Tyson S., Furman, Michael D. (2005). *Rapid Prototyping of Digital Systems,* 1st Edition or current edition. New York, NY: Klumer Academic
2. Floyd, Thomas (July 13, 2005). *Digital Fundamentals, 9th Edition or current edition.* Upper Saddle Hill, NJ: Pearson Education

Specific, *Measurable* Student Behavioral Learning Objectives:
Upon completion of this course the student should be able to:

1. Design, build and troubleshoot complex logic circuits within a team environment, utilizing digital Integrated Circuit (IC) technology and PLD hardware.
2. Utilize integrated development environment that includes design and PLD software to implement complex digital logic circuits.
3. Independently design a complex logic circuit and present the circuit and findings in written and oral format.

Detailed Outline of Course Content (Major Topics and Subtopics) **or Outline of Field Experience/Internship (experience, responsibilities and supervision):**

I. Programmable Logic Devices (PLD)
   A. Simple PLDs and Complex PLDs
   B. Altera CPLDs or Similar Devices
   C. Altera Macrocells or Similar Devices
   D. Altera MAX 7000 Family of CPLDs or Similar Devices

II. Programmable Logic Device Software
   A. Quartus II or Similar CAD System
   B. Initiating a PLD Project
   C. Schematic Design Entry
   D. Pin Assignment and Design Compilation
   E. Design Simulation

III. Programmable Logic Device Development Board
   A. Development Board Specification
   B. Development Board Resources
   C. Programming the Development Board PLD
   D. Testing and Troubleshooting the Designed PLD Circuit

IV. Counters
   A. Asynchronous Counters
   B. Synchronous Counters
   C. Up/Down Counters
   D. Design of Unique Sequence Counters
   E. Cascaded Counters
   F. Counter Applications

V. Shift Registers
   A. Serial In / Serial Out Shift Registers
   B. Serial In / Parallel Out Shift Registers
   C. Parallel In / Serial Out Shift Registers
   D. Parallel In / Parallel Out Shift Registers
   E. Bi-directional Shift Registers
   F. Shift Register Applications

VI. Memory Devices
   A. Semiconductor
   B. Magnetic
   C. Optical

Evaluation of Student Performance:
1. Written Exams
2. Written Lab Reports
3. Written Assignments
4. Design Demonstrations
5. Final Report and Presentation