(91)

September 27, 2012

METROPOLITAN STATE COLLEGE *of* DENVER
Office of Academic Affairs

REGULAR COURSE SYLLABUS

School of: Letters, Arts and Sciences

Department: Mathematical and Computer Sciences

Prefix & Course Number: CS 1400 **Crosslisted With*:** ____

Course Title: Computer Organization 1

Check All That Apply: Required for Major: X Required for Minor: ____ Specified Elective:

Required for Concentration: ____ Elective: X Service Course: ____

Credit Hours: 4 (4+0)

Total Contact Hours per semester (assuming 15-16 week semester):

Lecture 60 Lab 0 Internship 0 Practicum 0 Other (please specify type and hours): 0

Schedule Type(s): L **Grading Mode(s):** L

Restrictions (Variable Topics Course): ____

Prerequisite(s): An intermediate algebra course or one and one-half years of secondary school algebra or equivalent and appropriate score the mathematics preassessment placement test or higher level math course with a grade of "C" or better
Corequisite(s): none
Prerequisite(s) or Corequisite(s): ____

Banner Enforced:

Prerequisite(s): A02 FOR MIN. SCORE OF 22 OR S02 FOR MIN. SCORE OF 500 OR (52 FOR MIN. SCORE OF 090 AND 54 FOR MIN. SCORE OF 022) OR (52T FOR MIN. SCORE OF 090 AND 54 FOR MIN. SCORE OF 022) OR (52 FOR MIN. SCORE OF 090 AND 54T FOR MIN. SCORE OF 022) OR (52T FOR MIN. SCORE OF 090 AND 54T FOR MIN. SCORE OF 022) OR MAT 099 FOR LEVEL UG WITH MIN. GRADE OF C OR MAT 099 FOR LEVEL UG WITH MIN. GRADE OF T OR MTH 1110 FOR LEVEL UG WITH MIN. GRADE OF C OR MTH 1110 FOR LEVEL UG WITH MIN. GRADE OF T OR MTH 1400 FOR LEVEL UG WITH MIN. GRADE OF C OR MTH 1400 FOR LEVEL UG WITH MIN. GRADE OF T OR MTH 1410 FOR LEVEL UG WITH MIN. GRADE OF C OR MTH 1410 FOR LEVEL UG WITH MIN. GRADE OF T OR MTH 2410 FOR LEVEL UG WITH MIN. GRADE OF C OR MTH 2410 FOR LEVEL UG WITH MIN. GRADE OF T

Corequisite(s): ____
Prerequisite(s) or Corequisite(s): ____

Catalog Course Description:
In this course students will study the internal organization, characteristics, performance and interactions of a computer system's functional components. Binary codes and binary arithmetic, digital logic, central processor organization, instruction set architecture, input/output fundamentals and memory architecture are covered.

APPROVED:

Department Curriculum Committee	1-24-13 Date
Department Chair **OR** Program Director	1-24-13 Date
Dean **OR** Associate Dean	1/24/13 Date
Associate VP, Academic Affairs	2/28/13 Date

*If crosslisted, attach completed Course Crosslisting Agreement Form

Prefix and Course Number: CS 1400 September 27, 2012, 2012

Required Reading and Other Materials will be equivalent to:
Clements Alan. (2006). *The Principles of Computer Hardware, 4th edition.* New York, NY: Oxford University Press

Specific, *Measurable* Student Behavioral Learning Objectives:
Upon completion of this course the student should be able to

1. Convert numerical data from one format to another.
2. Perform binary arithmetic operations.
3. Use AND, OR, NOT, and XOR logical elements in the design of combinational and sequential logical circuits.
4. Describe instruction set architecture and the functionality of the central processing unit.
5. Describe input/output organization and how interrupts are used to implement input/output control and data transfers.
6. Discuss various bus technologies and compare their features and performance.
7. Explain the cost/performance tradeoffs of the memory hierarchy.

Detailed Outline of Course Content (Major Topics and Subtopics) **or Outline of Field Experience/Internship (experience, responsibilities and supervision)**

I. Data Representation and Digital Logic
   A. Binary representation of data
   B. Binary signed and unsigned arithmetic
   C. Range, precision, and errors in floating-point arithmetic
   D. Introduction to digital logic (logical elements, flip-flops)
   E. Boolean algebra and logical expressions
   F. Design of logical circuits

II. Computer Architecture and Organization
   A. Overview of the history of the digital computer
   B. Introduction to instruction set architecture and system architecture
   C. Processor architecture – instruction types, memory addressing modes, register sets, arithmetic logic unit
   D. Processor structures – memory-to-register, load/store, stack and acumulator processors

III. Interfacing and Input/Output Strategies
   A. Input/Output fundamentals: spinning (polling) and interrupt modes
   B. Interrupt mechanisms: vectored and prioritized, interrupt acknowledgment and masking
   C. Buses: bus transactions and protocols, bus arbitration

IV. Memory Architecture
   A. Primary, secondary and tertiary memories and their technologies
   B. Memory hierarchy, latency and throughput

Evaluation of Student Performance

A combination of the following:

1. Homework Assignments
2. Quizzes and Examinations
3. Final examination

Written communication skills will be applied in this course.

Prefix and Course Number: CS 1400 September 27, 2012

Program Student Learning Outcomes Assessment

Students should achieve the Program Student Learning Outcomes (Program SLOs) by the time of graduation. Each individual Program SLO is assessed by selecting one or more course SLOs that contribute to the evaluation of that one Program SLO.

1. Program SLO i: An ability to use current techniques, skills, and tools necessary for computing practices.
   Course SLO #4: Describe instruction set architecture and the functionality of the central processing unit.
   Course SLO #7: Explain the cost/performance tradeoffs of the memory hierarchy.

2. Program SLO j: An ability to apply mathematical foundations, algorithmic principles, and computer science theory in the modeling and design of computer-based systems in a way that demonstrates comprehension of the tradeoffs involved in design choices.

   Course SLO #1: Convert numerical data from one format to another.
   Course SLO #2: Perform binary arithmetic operations.
   Course SLO #3: Use AND, OR, NOT, and XOR logical elements in the design of combinational and sequential logical circuits.

3. Program SLO k: An ability to apply design and development principles in the construction of software systems of varying complexity.

   Course SLO #5: Descibe input/output organization and how interrupts are used to implement input/output control and data transfers.
   Course SLO #6: Discuss various bus technologies and compare their features and performance.