(51)

METROPOLITAN STATE UNIVERSITY OF DENVER
Office of Academic and Student Affairs

REGULAR COURSE SYLLABUS

College of: Professional Studies

Department: Engineering and Engineering Technology

Prefix & Course Number: CPE 4020 **Crosslisted With*:** _____

Course Title: Digital Systems III – Hardware Description Language

Transcript Course Title (30 characters): Digital Systems III

Check All That Apply: Required for Major: X Required for Minor:_____ Specified Elective: _____

Required for Concentration: _____ Elective: _____ Service Course: _____

To receive Title IV financial aid funds, all institutions of higher education must comply with the federal definition of a credit hour. The Higher Learning Commission requires institutions to maintain policies and procedures for verifying compliance with this definition.

> ***Federal Credit Hour Definition:*** *A credit hour is an amount of work represented in intended learning outcomes and verified by evidence of student achievement that is an institutionally-established equivalency that reasonably approximates not less than:*
> *(1) one hour of classroom or direct faculty instruction and a minimum of two hours of out-of-class student work each week for approximately fifteen weeks for one semester or trimester hour of credit, or ten to twelve weeks for one quarter hour of credit, or the equivalent amount of work over a different amount of time; or (2) at least an equivalent amount of work as required in paragraph (1) of this definition for other activities as established by an institution, including laboratory work, internships, practica, studio work, and other academic work leading toward to the award of credit hours. 34CFR 600.2 (11/1/2010)*

Credit Hours: 3 (2+2) **Schedule Type**: B **Grade Mode**: L

Face-to-Face or Equivalent Hours per course:

Lecture 30 Lab 30 Internship _____ Practicum _____ Other (please specify type and hours):_____

Additional Student Work Hours per course: 90

Variable topics umbrella course: No X **Yes** _____ If yes, number of credits/repeats allowed _____

Specified repeatable course: No X **Yes** _____ If yes, number of credits/repeats allowed _____

Prerequisite(s): CPE 2350 and CPE 3330 (with a grade of "C" or better for all prerequisites)

Corequisite(s): _____

Prerequisite(s) or Corequisite(s): _____

APPROVED:

Department Chair **OR** Program Director Date

Dean **OR** Associate Dean Date

Associate VP, Academic and Student Affairs Date

*If crosslisted, attach completed Course Crosslisting Agreement Form

Prefix and Course Number:

Banner Enforced Coding:

Prerequisite(s): CPE 2350 and CPE 3330 (with a grade of "C" or better for all prerequisites)
Corequisite(s): _____
Prerequisite(s) or Corequisite(s): _____

Registration restrictions: Level _____ **Class** _____**Program/Major** _____ **Student attribute** _____

Catalog Course Description:
This course covers a Hardware Description Language (HDL) which is used to design and simulate very large scale digital integrated circuits.

Specific Variable Topics Course Description (if applicable, umbrella course description included above):

Required Reading and Other Materials will be equivalent to:
Palnitkar, Samier (2003). *Verilog HDL 2nd edition* or current edition. Upper Saddle Hill, NJ: Prentice Hall.

Specific, *Measurable* Student Behavioral Learning Objectives:
Upon completion of this course the student should be able to:
1. Use a Hardware Description Language (HDL) to emulate hardware logic gate operation, establish data flows and model desired logic behavior
2. Simulate hardware designs using HDL and verify the results
3. Synthesize and test designs on Programmable Logic Device (PLD) hardware

Detailed Outline of Course Content (Major Topics and Subtopics) **or Outline of Field Experience/Internship (experience, responsibilities and supervision)**:

I. Gate, Dataflow and Behavioral Level Modeling and Simulation
   - A. Combinatorial Circuits
   - B. Registered Logic such as Registers and Counters
   - C. Finite State Machines

II. Simulation and Testing Designs
   - A. Waveform simulation
   - B. Writing Test Benches with HDL
     1. HDL Programming Structures for Simulation
     2. Topics in Verification and Simulation

III. PLD Synthesis of HDL designs
   - A. Synthesis tools and writing efficient logic for the PLD
   - B. Timing Closure
   - C. Constraints Management

IV. Course Projects
   - A. Implement a logic design project
   - B. Verify operation with simulation
   - C. Demonstrate operation to the class

Evaluation of Student Performance:
1. Lab Reports
2. Examinations
3. Written Assignments
4. Project Presentations